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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,961	12/05/2001	Jason G. Sandri	2207/12035	1389
23838	7590	12/19/2006	EXAMINER	
KENYON & KENYON LLP 1500 K STREET N.W. SUITE 700 WASHINGTON, DC 20005			TRUONG, CAMQUY	
			ART UNIT	PAPER NUMBER
			2195	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		12/19/2006	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/001,961	SANDRI ET AL.
	Examiner	Art Unit
	Camquy Truong	2195

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 15 November 2006.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-5, 10-15 and 18-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-5, 10-15 and 18-22 is/are rejected.

7) Claim(s) 23 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

1. Claims 1-5, 10-15, 18-23 are presented for examination.
2. It is noted that although the present application does contain line numbers in the specification and claims, the line numbers in the claims do not correspond to the preferred format. The preferred format is to number each line of every claim, with each claim beginning with line 1. For ease of reference by both the examiner and Applicant all future correspondence should include the recommended line numbering.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 22 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Prevent a failing logical processor from retaining a lock on the semaphore register is not disclosed in the specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5, 10-15, and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable Hays, Jr. et al. (U.S. Patent 4,354,227) in view of Forman et al (5,544,353).

6. As to claim 1, Hays teaches the invention substantially as claimed including: a method for controlling access to resources shared among a plurality of processors (1-2, Fig.1; col.1, lines 60-67), comprising

resource descriptor describing a usage allocation of resources shared among a plurality of logical processors (a control register for storing register indication of current state of availability of each resource, col. 10, lines 9-14, and lines 22-28);

obtaining exclusive access for said first logical processor to said resource file (col.5, lines 32-37);

Query resource descriptor to determine whether resources needed by said first processor is available (col.4, lines 24-27; col.5, lines 32-35; col. 10, lines 20-21);

If resources needed by said first processor are available, updating said resource descriptor to reserve said resources for exclusive use by said first processor (col. 5, lines 35-36; col. 6, lines 3-6; col. 10, lines 22-27); and

Releasing said exclusive access for said first processor to said resource descriptor (col. 10, lines 29-45).

7. Hays does not explicitly teach for a first logical processor, obtaining a lock on a semaphore controlling exclusive access to a resource descriptor, and obtaining exclusive access for said first logical processor to said resource file, if said lock is obtained. However, Forman teaches obtaining a lock on a semaphore controlling exclusive access to a resource descriptor if said lock is obtained (if access denied (resource file is locked and access by other processor, waiting and retrying until exclusive access to file is obtained, col. 6, lines 9-11. It obvious that Forman teaches that in order to exclusive access to resource file, it has to use the semaphore method to obtain the lock before accessing to share resource file), and obtaining exclusive access for said first logical processor to said resource file, if said lock is obtained (col. 5, lines 8-14; col. 6, line 13).

8. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Hays and Forman because Forman's obtaining exclusive access for a first processor to a resource descriptor, and obtaining exclusive access for said first logical processor to said resource file, if said lock is

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obtained would increase the efficiency of Hays's system by providing the step of obtaining exclusive access for a first processor to a resource descriptor, and obtaining exclusive access for said first logical processor to said resource file, if said lock is obtained to improve the efficiency using the share resource among a plurality of logical processors.

9. As to claim 2, Hays teaches if said resources needed by said first logical processor are not available, releasing said exclusive access for said first logical processor to said resource descriptor (col.5, lines 57-66).

10. As to claim 3, Hays teaches after the releasing, accessing a shared resource by said first logical processor (col. 10, lines 39-45).

11. As to claim 4, Hays teaches:

Query resource descriptor to determine whether resources needed by said second logical processor is available (col.4, lines 24-27; col.5, lines 32-35; col. 10, lines 20-21);

If resources needed by said second processors are available, updating said resource descriptor to reserve said resources for exclusive use by said second processor (col. 5, lines 35-36; col. 6, lines 3-6; col. 10, lines 22-27);

Releasing said exclusive access for said second processor to said resource descriptor (col. 10, lines 29-45); and

Forman teaches obtaining access for a second processor to a resource descriptor describing a usage allocation of said shared resources (col. 2, lines 33-41; col. 5, lines 3-9; col. 6, lines 3-10).

12. As to claim 5, Hays teaches if said resources needed by said second logical processor are not available, releasing said exclusive access for said second logical processor to said resource descriptor (col.5, lines 57-66).

13. As to claim 10, Hays teaches:

A plurality of logical processors (1-2, Multiprocessor A, Multiprocessor B, Fig.1, col. 1, line 64);

A plurality of resources shared by said plurality of logical processors (col. 1, lines 59-64);

A resource descriptor to identify a status of said shared resources (col. 10, lines 9-13); and

A semaphore to control access by said plurality of logical processors to said resource descriptor (col. 2, lines 8-12; col. 10, lines 16-19).

14. As to claim 11, it is rejected for the same reason as claim 6.

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15. As to claim 12, it is rejected for the same reason as claim 11. In addition, Hays teaches first and second processors concurrently use first and second resources (col. 1, lines 7-16; col. 7, lines 55-61).

16. As to claim 13,

Hays teaches:

Generating a first bitmap identifying said first required resource (col. 5, lines 35-36; col. 6, lines 3-6; col. 10, lines 22-27), and using first resource (col. 10, lines 43-45);

Applying said first bitmap to said resources descriptor register to reserve said first require resource (col. 5, lines 35-36; col. 6, lines 3-6; col. 10, lines 22-27).

Forman teaches:

setting a lock bit in a semaphore register to reserve exclusive access to resource descriptor register (write a master process identification information, wherein each processes having a separate address space, to share resources control file, col. 2, lines 33-41; col. 3, lines 15-18; col. 5, lines 3-9; col. 6, lines 3-10); and re-setting semaphore lock bit to release exclusive access (col. 2, lines 7-10; col. 6, lines 53-57).

17. As to claim 14, it is rejected for the same reason as claim 13. In addition, Hays teaches first and second processors use first and second resources in parallel (col. 1, lines 7-16; col. 7, lines 55-61).

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18. As to claim 15, Hays teaches setting a lock bit comprises supplying an identifier of said first logical processor for writing into said semaphore register (col. 2, lines 20-21; col. 6, lines 3-11; col. 6, line 66-col.7, line 4).

19. As to claim 18, it is rejected for the same reason as claim 1.

20. As to claim 19, Hays teaches resource descriptor includes a plurality of fields each to associate a resource with a logical processor identifier (col. 10, lines 22-28).

21. As to claim 20, it is rejected for the same reason as claim 1. In addition, Hays teaches

Determine whether a need resource is available based on said resource descriptor (col. 5, lines 32-37; col. 10, lines 22-28),

If so, reserve the resource (col. 2, lines 26-30).

Forman teaches:

Obtain a lock on said semaphore register to reserve exclusive access to resource descriptor (if access denied (resource file is locked and access by other processor, waiting and retrying until exclusive access to file is obtained, col. 6, lines 9-11. It obvious that Forman teaches that in order to exclusive access to resource file, it has to use the semaphore method to obtain the lock before accessing to share resource file);

Release the lock on the semaphore register (col. 6, lines 53-54).

22. As to claim 21, Hays teaches reserving one or more resource by assigning a logical processor identifier to corresponding resource (col. 10, line 22-28, and lines 43-45).

23. Claim 22 are rejected under 35 U.S.C. 103(a) as being unpatentable Hays, Jr. et al. (U.S. Patent 4,354,227) in view of Forman et al (5,544,353), and further in view of Lee et al. (U.S. Patent 5,421,002).

24. As to claim 22, Hays and Forman do not explicitly teach preventing a failing logical processor from retaining a lock on the semaphore register. However, Lee teaches preventing a failing logical processor from retaining a lock on the semaphore register (col. 4, lines 27-29).

25. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Hays, Forman and Lee because Lee's preventing a failing logical processor from retaining a lock on the semaphore register would improve the data integrity of Hays and Forman's system by providing the step of preventing a failing logical processor from retaining a lock on the semaphore register to enable operation to continue even if one component fails.

Allowable Subject Matter

26. Claim 23 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

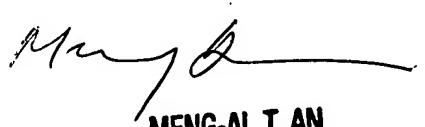
27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Camquy Truong whose telephone number is (571) 272-3773. The examiner can normally be reached on 8AM – 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-3756.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIP. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIP system, contact the Electronic Business Center (EBC) at 866-217-9197(toll-free).

Camquy Truong

November 27, 2006


MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100